Q.P. Code: 16EC408 **R16**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech II Year II Semester Supplementary Examinations July-2021

COMPUTER ORGANIZATION AND ARCHITECTURE

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	a	Explain the basic components of Generic Computing system regardless of its internal architecture with practical real time examples.	7M
	b	Write about hierarchy of buses, bus signals and its functionalities.	5M
		OR	
2	a	Demonstrate how the Compatibility between CPU & Bidirectional IO components are devised using its interfacing modules.	6M
	b	List out the features of different levels in computer programming languages?	6M

UNIT-II

3	a	Write about Interrupt and its types?	6M
	b	Illustrate the phases of Interrupt Cycle with a neat flowchart.	6M
		OR	
4	a	Design hardware for signed magnitude addition and subtraction?	6M
	b	Explain the process for signed magnitude addition and subtraction with flow chart.	6M

UNIT-III

5	a	Design Bus system for Four-bit register using 4x1 Mux.	6M
	b	Implement Bus line for an 8-bit register using three state-buffers.	6M
		OR	
6	a	Why RTL is preferred for describing internal organization of digital computers.	4M
	b	Illustrate the register transfer mechanism for P: R2 R1 with necessary diagrams.	8M

UNIT-IV

7	a	What is virtual memory? Explain the relation between address space and memory space in a virtual memory system along with its memory table for mapping?	8M
	b	What is Locality of Reference and explain about Cache memory in detail.	4M
		OR	
8	a	Explain Virtual address Mapping using Pages with necessary examples.	6M
	b	Brief out the hardware organization of Associative memory with diagrams.	6M

UNIT-V

9	a	Classify organization of computers using Flynn's criteria.	6M
	b	Write about pipelining and its importance in high speed applications.	6M
		OR	
10	a	Implement a simple pipeline unit for floating addition and subtraction.	6M
	b	Consider an adder circuit with delays of four segment as t_1=60 ns, t_2=70 ns,t_3=100 ns,t_4=80 ns and interface resistors have a delay of t_r=10 ns. i) Find the clock cycle for pipeline. ii) Find out clock cycle for non-pipelined adder.	6M

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